Claims

What is claimed is:

[c1] A computer system, comprising:

a phase locked loop having a phase-frequency detector, wherein the phase-frequency detector inputs a system clock and generates a chip clock, and wherein the phase-frequency detector generates pulses on a first signal and second signal dependent on a relationship between the system clock and the chip clock; and

a lock detect indicator that uses the first and second signals to determine whether the phase locked loop is out of lock.

[c2] The computer system of claim 1, wherein the system clock is a system clock.

[c3] The computer system of claim 1, wherein the lock detect indicator comprises:

circuitry that generates a first lock indication pulse if a pulse on the first signal or second signal is longer than a predetermined pulse width;

circuitry that generates a second lock indication pulse dependent on the first lock indication pulse and a count value; and

circuitry that uses the second lock indication pulse to dynamically generate a lock status signal, wherein the lock status signal is indicative of whether the phase locked loop is out of lock.

[c4] The computer system of claim 1, wherein the lock detect indicator comprises:

circuitry that outputs another lock status signal, wherein the another lock status signal is indicative of whether the phase locked loop is out of lock.

[c5] The computer system of claim 1, wherein the lock detect indicator comprises:

circuitry that outputs a past lock status signal, wherein the past lock status

signal indicates whether the phase locked loop has been out of lock.

[c6] The computer system of claim 1, wherein the lock detect indicator comprises:

reset circuitry that resets the lock detect indicator dependent on a reset input signal.

[c7] An integrated circuit, comprising:

circuitry that generates a first lock signal dependent on a first signal and a second signal used in a clock generator;

circuitry that generates a lock reset signal dependent on the first lock signal and a reset input signal;

circuitry that generates a second lock signal dependent on the lock reset signal; and

circuitry that outputs a lock status signal dependent on the second lock signal.

[c8] The integrated circuit of claim 7, wherein the clock generator is a phase locked loop.

[c9] The integrated circuit of claim 7, wherein the circuitry that outputs the lock status signal is dynamic.

[c10] The integrated circuit of claim 7, wherein the clock generator comprises:

a phase detector that inputs a system clock and a chip clock, wherein the phase detector generates the first signal and the second signal dependent on a phase relationship between the system clock and the chip clock.

[c11] The integrated circuit of claim 10, wherein the phase detector generates a pulse on the first signal when a phase of the system clock lags behind a corresponding phase of the chip clock, and wherein the phase detector generates a pulse on the

second signal when a phase of the chip clock lags behind a corresponding phase of the system clock.

[c12] The integrated circuit of claim 10, further comprising:

circuitry that generates a clock generator pulse signal dependent on the system clock, chip clock, and the second lock signal.

[c13] The integrated circuit of claim 7, wherein the circuitry that generates the first lock signal comprises:

delay circuitry having a predetermined delay; and

circuitry that generates a pulse on the first lock signal when a pulse on the first signal or the second signal is greater than the predetermined delay.

[c14] The integrated circuit of claim 7, wherein the circuitry that generates the lock reset signal comprises:

circuitry that removes glitches on the first lock signal;

circuitry that amplifies a pulse on the first lock signal; and

circuitry that uses the pulse on the first lock signal to selectively reset the circuitry that generates the second lock signal.

[c15] The integrated circuit of claim 7, wherein the circuitry that generates the lock reset signal is dependent on a reset input signal.

[c16] The integrated circuit of claim 7, wherein the circuitry that generates the second lock signal comprises:

counter circuitry that counts to a particular value; and

circuitry that generates a pulse on the second lock signal when the counter circuitry reaches the particular value.

[c17] The integrated circuit of claim 7, further comprising:

circuitry that generates a past lock signal dependent on the second lock signal, wherein the past lock signal indicates whether the clock generator has been out of lock.

[c18] An integrated circuit, comprising:

generating means for generating a chip clock signal based on a system clock signal, wherein the generating means uses a first signal and a second signal to maintain a relationship between the chip clock and the system clock;

detecting means for using the first and second signals to determine whether the generating means is out of lock; and

indicating means for indicating whether the generating means is out of lock.

[c19] A method for detecting whether a phase locked loop is out of lock, comprising:

determining whether a pulse of a first signal or a second signal used in the phase locked loop is greater than a predetermined width;

generating a pulse on a first lock signal based on the determination; and

dynamically generating a pulse on a lock status signal dependent on the pulse on the first lock signal.

[c20] The method of claim 19, wherein the phase locked loop comprises a phase detector that inputs a system clock and a chip clock, wherein the phase detector generates the first signal and the second signal dependent on a phase relationship between the system clock and the chip clock.

[c21] The method of claim 20, wherein the phase detector generates a pulse on the first signal when a phase of the system clock lags behind a corresponding phase of the chip clock, and wherein the phase detector generates a pulse on the second signal when a phase of the chip clock lags behind a corresponding phase of the system clock.

[c22] The method of claim 20, further comprising:

generating a pulse signal of the phase locked loop dependent on the system clock and the pulse on the first lock signal.

[c23] The method of claim 19, wherein generating the first lock signal comprises:

using a predetermined delay; and

generating the pulse on the first lock signal when a pulse on the first signal or the second signal is greater than the predetermined delay.

[c24] The method of claim 19, further comprising generating a lock reset signal, wherein generating the lock reset signal comprises:

removing glitches on the first lock signal;

amplifying the pulse on the first lock signal; and

using the pulse on the first lock signal to selectively reset circuitry used for generating a second lock signal.

[c25] The method of claim 24, wherein generating the lock reset signal is dependent on a reset input signal.

[c26] The method of claim 24, wherein generating the second lock signal comprises:

counting to a particular value; and

generating a pulse on the second lock signal when circuitry used for counting to the particular value reaches the particular value.

[c27] The method of claim 24, further comprising:

generating a pulse on a past lock signal dependent on the second lock signal, wherein the past lock signal indicates whether the phase locked loop has been out of lock.